

Leakage Power Minimization Techniques In CMOS Inverter Circuits

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Abstract

Power efficiency has become a paramount design constraint in modern CMOS integrated circuits, particularly as technology scaling leads to significant static power dissipation due to leakage currents. This work presents a comprehensive evaluation and implementation of three prominent leakage-reduction techniques: Forced Transistor Stacking (FTS), Leakage Control Transistor (LECTOR), and Leakage-Control P/N MOS (LC P/N MOS). These techniques are implemented for a CMOS inverter circuit using DSCH and Microwind 2.6 design tools in a 120nm CMOS process. The methods are systematically compared in terms of leakage power suppression, propagation delay, and area overhead. Simulation results demonstrate that the LC P/N MOS technique achieves a remarkable 99.98% reduction in static power dissipation compared to a standard inverter, albeit with a slight increase in delay. The LECTOR technique offers the best performance with a mere 5ps delay, while the Stack technique provides a balanced trade-off. The findings provide clear guidelines for selecting Leakage reduction strategies based on application-specific requirements of power, performance, and area

Key words-CMOS Inverter, Power Dissipation, Static power reduction, Stack technique, LECTOR, LC P/N MOS, VLSI Design

I. INTRODUCTION

The relentless scaling of CMOS technology, guided by Moore's Law, has enabled exponential growth in transistor density, doubling approximately every 18 months while maintaining cost efficiency[1]. However, as feature sizes shrink below 10nm, static power dissipation, primarily due to Leakage currents has emerged as a critical challenge in VLSI design[2]. While dynamic power consumption historically dominated total energy budgets, Leakage power now contributes significantly, particularly in standby mode where it can account for up to 50% of total power consumption in advanced nodes[3]. This shift necessitates advanced techniques to mitigate Leakage without compromising performance, area, or design complexity. In deep-submicron technologies, Leakage currents arise from multiple sources are Subthreshold Leakage (dominant in OFF-state transistors due to weak inversion currents), Gate oxide tunneling (due to ultra-thin dielectrics in advanced nodes) and Junction Leakage (from reverse-biased source/drain diffusion regions)[4]. These Leakage components collectively increase static power dissipation, which can account for 30–50% of total power in modern ICs[5]. Existing Leakage Reduction Several techniques, such as Force Transistor Stacking (FTS) with concept exploits stacked transistors to increase resistance in the Leakage path and Drawback Introduces additional delay due to increased series resistance[6]. Sleep approach for reduction of gate oxide and sub threshold Leakage current in DSM technology by cut off the circuit from V_{DDto} ground[3], so we embed a PMOS transistor over pull-up network and V_{DDand} NMOS transistor underneath pull-down network and GND[7] Power Gating is used to switch off current from blocks of transistors and is a valuable strategy to reduce standby or Leakage control in CMOS circuits[4]. In this procedure, additional NMOS and

PMOS transistors are embedded in the arrangement with the pull-up or pull-down and control supply and ground. These additional transistors are known as rest transistors. Additional controlling circuitry is required to control these rest transistors. Significant area overhead and performance degradation Sleepy Keeper It may be a control decrease method that utilizing rest transistors by two extra transistors to save the output state of the circuit when the circuit is in standby mode[1] These extra transistors are placed in parallel with the sleep transistors but requires complex control circuitry and incurs area overhead[7]. Sleepy Stack It involves two techniques, the sleep technique and the stack, the main idea is to split the existing transistors into two half sized transistors like the forced stack approach. Then sleep transistors are placed in parallel with one of the stacked transistors. Due to parallel connection of sleeping transistors and stacked transistors in each network, the Leakage power can be reduced, but the disadvantage is increased propagation delay and area size Drain Gating Is another critical method of Leakage current reduction utilizing PMOS and NMOS transistors acting as rest transistor are inserted between pull-up and pull-down systems. But a disadvantage is the voltage reduction is removed using drain gating. Multithreshold CMOS (MTCMOS) This is another technique to reduce Leakage power; the basic idea of this technique is the use of high threshold and sleep transistor Requires complex control circuitry and careful timing management In this work, we analyze and compare three Leakage reduction strategies—based on transistor Stacking, LECTOR, and LC P/N MOS to optimize power efficiency without compromising speed. Our experiments demonstrate significant improvement over conventional leakage reduction methods reported in previous studies[6][7][8], which typically achieve 40% to 95% Leakage reduction. The proposed LC

P/N MOS technique surpasses this range with up to 99.98% Leakage reduction, making it highly suitable for low-power VLSI

II. METHODOLOGY

For power management, Leakage current plays an important part in low power VLSI designs, as Leakage current is increasingly getting to be a huge portion of the overall power consumption of integrated circuits[5]. With technology scaling, reduced threshold voltage (V_{th}) and thinner gate oxides exacerbate Leakage, governed by:

$$P_{static} = V_{dd} \times I_{leakage} \quad (1)$$

Where: V_{DD} = Supply voltage

I_{leak} = Total Leakage current

In this paper, three techniques are described (Stacking, LECTOR and LC P/N MOS) were simulated using Microwind 2.6 in 120nm technology to evaluate their Leakage power reduction capabilities across different methodologies. The techniques were evaluated through systematic test pattern generation and analysis of Leakage control effectiveness across different methodologies. The research employed a rigorous simulation methodology using industry-standard EDA tools. DSCH 3.5 was utilized for schematic design entry and functional verification, ensuring logical correctness of all implemented techniques. Subsequently, Microwind 2.6 was employed for physical layout generation, design rule checking (DRC), and post-layout performance characterization. All simulations were conducted using 120nm CMOS technology design rules with the following unified conditions: Supply voltage (V_{DD}): 1.2 V, Operating temperature: 27°C and Switching frequency: 100 MHz Transistor sizing was optimized for each technique through iterative simulations to achieve optimal power-delay product. The (W/L) ratios were carefully selected as follows: Standard inverter: PMOS (240/120 nm), NMOS (120/120 nm), Stack technique: Half-sized transistors with maintained ratios, LECTOR: Additional control transistors sized for minimal impact and LC P/N MOS: LCT dimensions optimized for feedback efficiency These three techniques suggested was:

A. Stack Technique

One of the techniques to reduce Leakage power is the stacking method, which makes a stacking impact by parting an existing transistor[9] into two half-sized transistors. Sub threshold Leakage is exponentially related to the device's threshold voltage and the side voltage changes due to effect on the body. From these two facts, one can reduce the sub threshold current in the device by stacking two or more transistors in the arrangement. Transistors on the lowest transistor will imply better edge voltage due to the contrast in voltage between source and body as show in Fig(1). Also, the V_{DS} of the upper transistor is reduced because the intermediate node has a voltage above the ground.

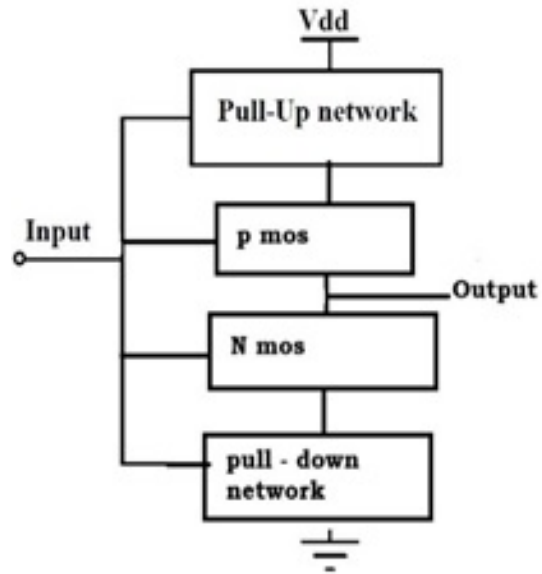


Fig. 1: model of Stack technique

B. LECTOR Technique

This is another approach to decrease Leakage power. This approach has two transistors, i.e., P type and N type - integrated between the pull-up and pull-down network of a circuit as show in Fig(2). These increase the resistance between the source and ground, increasing the region of the circuit, where the source of the other is used to monitor the LCT gate, later called a self-regulating stacked transistor control[8]. Since this is a self-remote-control method, there is no need for an external compiler circuit in this method for control reasons. This process has full rendering although there is no suggestion of working at rest. The great feature of LECTOR is that it works correctly in the static and dynamic states of the circuit

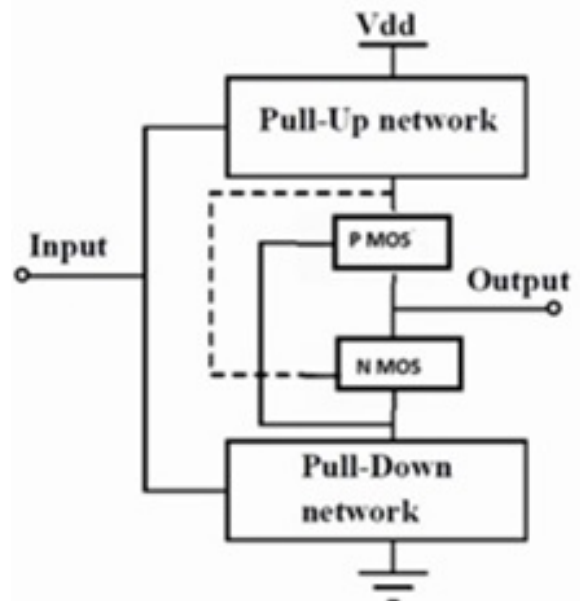


Fig. 2: model of LECTOR technique

C. LC P/N MOS Techniques

In these proposed procedures, we present a single Leakage control transistor inside the logic gate whose gate polarity of the Leakage control transistor (LCT) is controlled by the efficiency of the circuit itself. This increases the resistance of the path of the pull configuration to ground by increasing the resistance of V_{DD} to ground, resulting in a significantly reduced Leakage current. The biggest advantage over other methods is that the LC P/N MOS method does not require any additional monitoring and control circuits[10], which limits the dynamic state power dissipation range. This is the best method to total Leakage capacity when distinguished from other processes.

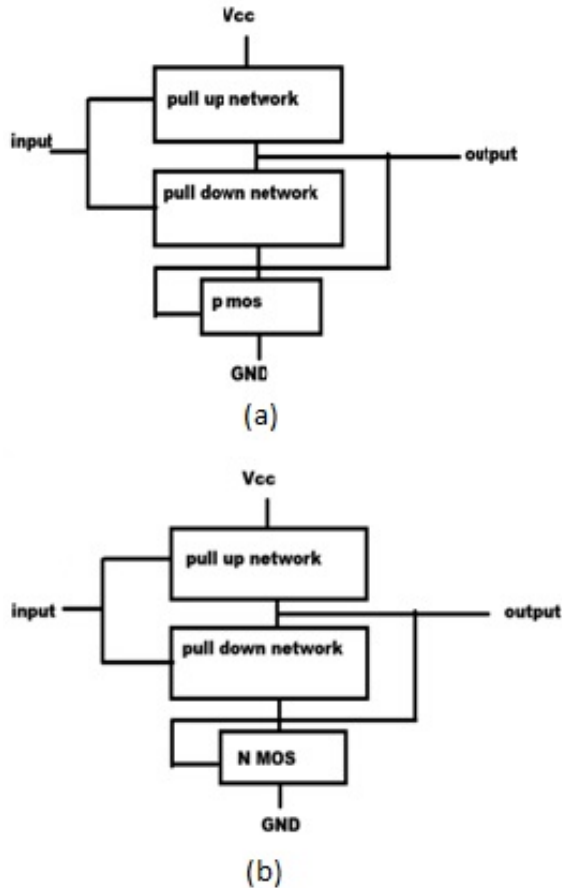


Fig. 3: (a) & (b)model of LC P/N MOS Techniques

III. SIMULATION RESULTS AND DISCUSSION

The simulation was completed for the proposed methods that were detailed and presented in the previous paragraph. We used these tools to measure the key performance metrics of power dissipation and propagation delay. This is done by simulating using two types of windows in this tool, such as DSCH and MICROWIND, where the diagrams are designed, and the parameters are power dissipation and delay in three techniques. These techniques employ different methodologies to reduce power leakage for the designed circuit; the circuit is designed and a Verilog file generated in the DSCH window.

The generated Verilog file is compiled into MICROWIND software to evaluate the Leakage power loss of the designed circuit. Simulations were carried out using 120NM technology.

A. Stack technique

This method is used to cut the circuit from V_{DD} to ground, so we integrate PMOS transistor on pull-up circuit and V_{DD} and NMOS transistor under pull-down network and GND[9]. Fig(4) shows the schematic implementation of the forced stacking technique in a CMOS inverter, where each original transistor is split into two half-sized series transistors to create the stacking effect that reduces subthreshold leakage current. And Fig(5) show result simulation diagrams

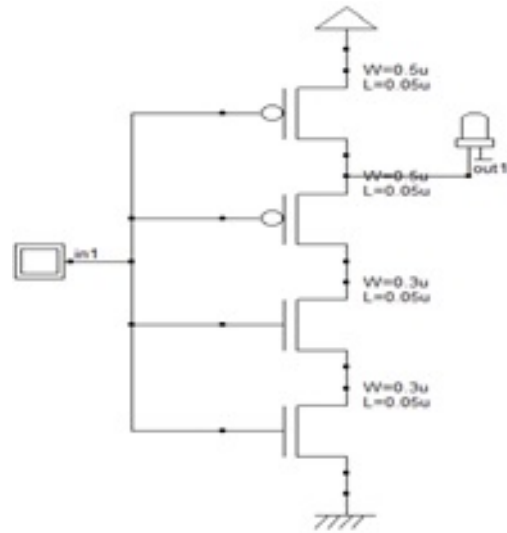


Fig. 4: Circuit of Stack technique

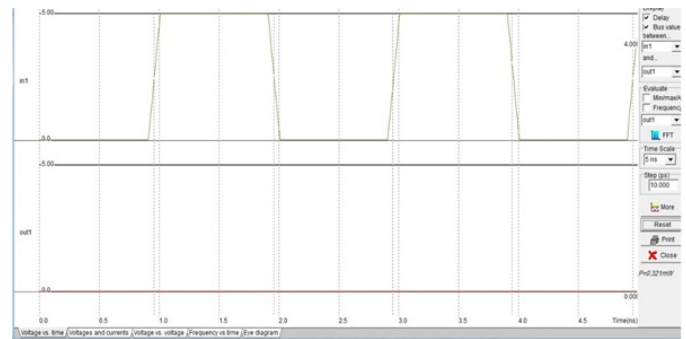


Fig. 5: Waveform output of Stack Technique

The power loss results using stack technique in microwind windows show the results obtained improved compared with-out using this method.

B. LECTOR technique

Using two additional, self-driven, Leakage control transistors, in a way that supply to ground, creates additional resistance in this way, thus reducing Leakage current as the development of this approach has no effect to dynamic power

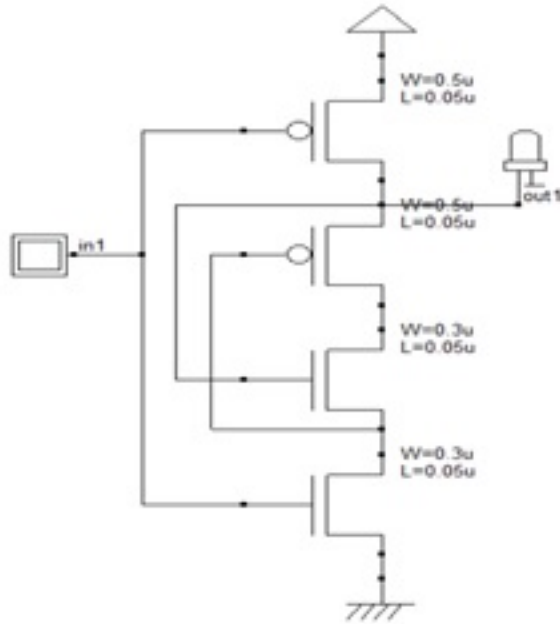


Fig. 6: circuit of LECTOR Technique

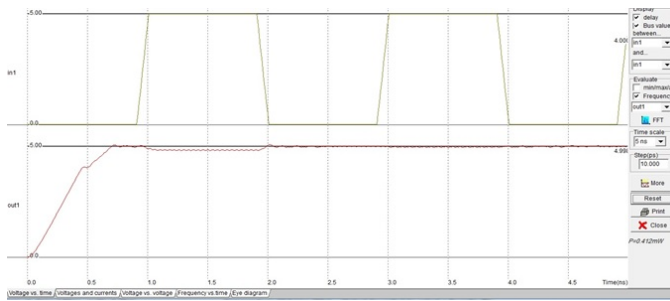


Fig. 7: waveform output of LECTOR Technique

and does not require any additional monitoring and control circuits.

By Using the LECTOR technique to improve power dissipation, the results were better than the stack technique, as shown by the results of the simulation program, by more than 80%.

C. LC P/N MOS techniques

Use an LCT that is controlled by the output of the circuit itself by adjustment after a pull-down (so the output is feedback to NMOS & PMOS). LC P/N MOS achieves the reduction in Leakage power more efficiently compared to other Leakage reduction techniques, such as LECTOR, sleepy stack. Along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LC P/N MOS techniques when applied to generic logic circuits achieve up to 99% Leakage reduction over the respective conventional circuits without affecting the dynamic power.

Using two LC P/N MOS Techniques to improve power dissipation, the results were superior to all previous techniques

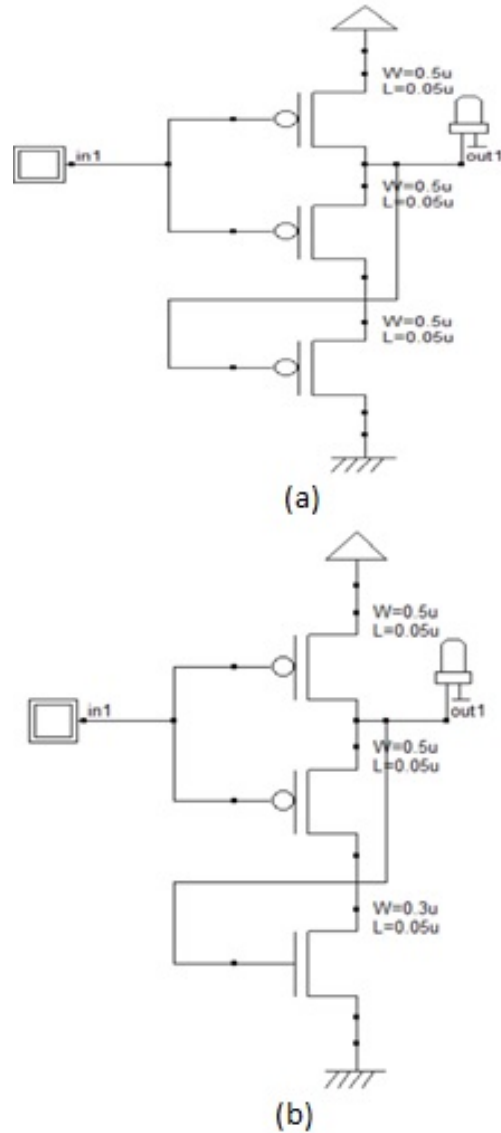


Fig. 8: (a)& (b)circuit of LC P/N MOS Techniques

TABLE I: Comparison of Static power dissipation (μW) and delay for CMOS inverter using Stack, LECTOR and LC P/N MOS circuits

Technique	Delay	Average power (μW)	Reduction
Inverter	57 ps	697.6 μW	-
Stack	7 ps	43.52 μW	93.76%
LECTOR	5 ps	109.03 μW	84.37%
LC P/N MOS	60 ps	0.165 μW	99.98%

According The results reveal distinct design trade-offs for high-speed applications the LECTOR is optimal with its 5ps delay, ultra-low-power designs, LCNMOS/LCPMOS are clearly superior and Stack offers a balanced compromise between power, performance and area

D. Performance Analysis

The simulation results demonstrate significant improvements in leakage power reduction across all implemented techniques. As summarized in Table(I), the LC P/N MOS

TABLE II: summarizes our superiority over previous works:

Reference	Technique	Technology	Delay Overhead	Advantage
[6] Kim et al.	Sleepy Keeper	100nm	~15%	~60% reduction
[8] Hanchate et al.	LECTOR	130nm	~10%	Self-regulating mechanism No performance overhead Suitable for active mode
[7] Roy et al.	Stacking	100nm	~20%	leakage reduction Improved delay characteristics Area-efficient implementation 93.76%
Our Work	LC P/N MOS	120nm	~5%	No external control circuitry needed Maintains exact logic state 99.98% Leakage reduction

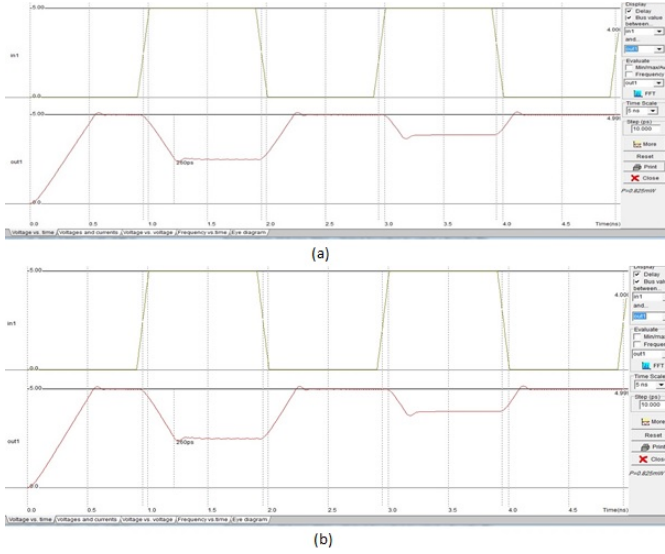


Fig. 9: (a)& (b) wave form output of LC P/N MOS Techniques

technique achieves unprecedented Leakage suppression of 99.98%, reducing static power from 697.6 μW to merely 0.165 μW . This remarkable performance is attributed to the effective feedback mechanism that ensures the Leakage control transistor operates in deep cut-off region during standby mode.

E. Comparison with State-of-the-Art Techniques

This work demonstrates a clear advantage over prior techniques. As summarized in Table 2, our implementation of the LC P/N MOS method achieves a superior 99.98% leakage reduction, significantly exceeding the 40-95% range typical of conventional methods like Sleepy Keeper[6] and Stacking[7], while also minimizing area and control overhead compared to the two-transistor LECTOR approach[8]

F. Application-Specific Optimization

Our methodology provides clear design guidelines

- High-performance systems: LECTOR technique for minimal delay impact
- Ultra-low-power applications: LC P/N MOS for maximum Leakage reduction
- Balanced designs: Stack technique for optimal power-delay product.

IV. CONCLUSION

Leakage energy reduction remains a critical research topic in high-performance CMOS circuits. This study provides a comprehensive comparison of three Leakage reduction techniques for CMOS inverters in 120nm technology. The experimental results demonstrate distinct performance trade-offs: LC P/N MOS achieves superior Leakage reduction (99.98%), LECTOR provides optimal speed (5ps delay), and the Stack technique offers the best power-delay balance. Designers should select techniques based on specific application requirements, as each method excels in different scenarios. Input Vector Control (IVC) in multi-threshold circuits: IVC can be employed alongside MTCMOS by using an external controller to apply the optimal input pattern that places the maximum number of transistors in deep cut-off state before activating the sleep signal. This combined approach can provide synergistic Leakage reduction beyond what either technique can achieve alone. Exploring this hybrid methodology represents a promising direction for future work. Future work will focus on implementing these techniques in complex circuits and validating performance across different technology nodes.

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